ABSTRACT OF THE DISCLOSURE

A technique for compensating for duty cycle distortion in an output data signal generated by a synchronous dynamic random access memory device (SDRAM) is provided. The output latch of the SDRAM is driven by an output clock signal generated by a delay lock loop (DLL). The output clock signal is phase-shifted relative to a reference clock signal received by the DLL such that the data removed from the output latch is synchronous with the reference clock signal. Further the duty cycle of the output clock signal is adjusted in a phase inverse relationship to the duty cycle distortion introduced by the output latch. As a result, the output data signal has reduced duty cycle distortion.